Synopsis V1.0
Proton SEE test of Gflx process from LSI Logic

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I. Introduction

This study was undertaken to determine the proton induced single event destructive and transient susceptibility of the LSI Logic Gflx standard process and two versions of Gflx radiation hardened process. The test vehicle is a logic chip. Device under test (DUT) was monitored for single event upset (SEU) and for destructive events induced by exposing it to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility.

II. Devices Tested

LSI Logic Gflx standard technology is a 0.11 μm CMOS bulk process. The two versions of the radiation-hardened process include a buried layer in order to guarantee SEL immunity.

The Logic chip test vehicle L9A0443 contains 384 64-bit ALU and 4 PRMNDM3 (process monitor) organized as 6 64 64-bit ALU modules (ALU_64_HD). In each module, the 64 ALUs share the same inputs and the output pass through a 64:1 output MUX tree. Each ALU (ALU_WRAP_HD) has a scan chain that connect the 200 flip-flop (operands a and b, outputs,…). Individual ALU outputs are only accessible through the scan chain. The power supply core voltage is 1.2V, and the I/O supply voltage is 3.3V. The Logic test vehicle is packaged in a cavity up 492 PBGA package (code I735).

The test samples' package markings are shown in table 1.

Table 1: logic chip test samples

Test vehicle	Process	Marking	SN#
L9A0443	Standard (bulk)	LSI Logic L9A0492 GAH15900.14 EEH27001.1 Control 24 G 0528 Δ Korea	1, 2
	Buried layer 1 (Dose 5)	LSI Logic L9A0492 GAH15900.14 EEH27001.3 1.6M5E14 12 G 0528 Δ Korea	33, 36
	Buried layer 2 (Dose 1)	LSI Logic L9A0492 GAH15900.14 EEH27001.2 1.6M1E14 7 G 0528 Δ Korea	17

III. Test Facility

Facility: Indiana University Cyclotron Facility (IUCF), Bloomington, IN
Energy: 200 MeV
Flux: 1 x 10^7 to 1 x 10^8 particles/cm^2/s depending on device sensitivity.
Fluence: All tests were run to 1 x 10^{10} p/cm^2 or until at least 100 SEU occurred.

IV. Test Conditions and Error Modes

Test Temperature: Room Temperature
Operating Frequency: 16 MHz
Power Supply Voltage: core: 1.2V, I/Os: 3.3V

PARAMETERS OF INTEREST: Power supply currents, device functionality

SEE Conditions: SEL, SEU, MEU, SET

V. Test Methods

Logic chip was tested with NASA-GSFC REAG (Radiation Effects and Analysis Group) Low Cost Digital Tester (LCDT). LCDT is a reusable universal digital device tester based on Xilinx Spartan 3 Field Programmable Gate Array (FPGA) with input/output (I/O) operation speed up to 200 MHz.
LCDT is the main test board that interfaces with the DUT-specific daughter card. The DUT on the daughter card is exercised using the configurable FPGA on LCDT with Hardware Design Language such as VHDL based coding. A remote PC controls LCDT.

During irradiation, DUT power supply currents (core and I/Os) are monitored. Nominal currents at 16 Mhz are 20 mA for I/Os and 380 mA for the core. As soon as on of the current reaches a programmable (500 mA for the core and 40 mA for the I/Os) SEL detection level, the DUT power supplies are shutdown.

Logic was tested in scan mode. In this mode, the device is functionally equivalent to 6 shift register chains of 200 flip-flops each. 5 out of the register chains were tested in parallel in the following way: a test pattern is entered in the chain input. The chain output is compared to the test pattern. Errors are counted and error information is stored (clock cycle#, chain number, read bit value, expected bit value). Two different test patterns were used: all0 and all1.

VI. Test Results

Test results are given in Table 2. No SEL or micro latchup were observed during the proton tests. The number of observed SEUs is very low. Maximum measured cross-section is 2 10^{-13} cm^2/flip-flop.

Table 2: proton SEE test results

Run #	Type	SN #	CLK speed (MHz)	Pattern	Energy (MeV)	Fluence (#/cm^2)	SEU #	Xsection (cm2/dev)
48	BL 1	36	16Mhz	ALL0	200	5.00E+09	1	2.00E-10
49	BL 1	36	16Mhz	ALL1	200	1.25E+09	0	0.00E+00
51	Bulk	2	16Mhz	ALL0	200	1.00E+10	0	0.00E+00
52	Bulk	2	16Mhz	ALL1	200	1.00E+10	0	0.00E+00
54	BL 2	17	16Mhz	ALLO	200	1.00E+10	1	1.00E-10
55	BL 2	17	16Mhz	ALL1	200	1.00E+10	0	0.00E+00
57	Bulk	1	16Mhz	ALL0	200	1.00E+10	2	2.00E-10
58	Bulk	1	16Mhz	ALL1	200	1.00E+10	0	0.00E+00
60	BL 1	33	16Mhz	ALLO	200	1.00E+10	0	0.00E+00
61	BL 1	33	16Mhz	ALL1	200	1.00E+10	0	0.00E+00

Reference documents:

- "Gflx PQV Logic Qchip," file L9A0492_des.pdf, Sep 19, 2002.
- "L9A0443, I735 package, pinout", file L9A0492.xls.
- "Low cost digital tester hardware manual," 2005.